R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR CLAIM AMENDMENTS

Claims 1 and 24 have been amended to include the limitations of claim 17. As such no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-25 under 35 U.S.C. §103 as being unpatentable over Levine et al. 5,970,439 (hereinafter Levine) is respectfully traversed and should be withdrawn.

Levine teaches performance monitoring in a data processing system (Title).

In contrast, claim 1 of the present invention provides an apparatus comprising a full system monitor. The monitor may be configured to (i) monitor in real-time (i) one or more software variables down to change rates, (ii) monitor in real-time one or more hardware registers down to cycle rates, (iii) monitor in real-time one or more firmware registers down to microcode fetch rates and (iv) monitor and calculate a frequency of use of each bit in one or more hardware register and one or more firmware registers in response to one or more trigger signals. The one or more trigger signals may be generated by a first comparator circuit.

Claim 24 provides similar limitations. Levine does not teach or suggest such a method or apparatus.

In particular, Levine fails to teach the presently claimed full system monitor configured to monitor in real time in response to a one or more trigger signals generated by a first comparator circuit. Levine is silent regarding a first comparator circuit configured to generate one or more trigger signals. The Office Action presents the new argument that "control registers . . . which would select events to count" (see Office Action page 3, line 16) is the presently claimed first comparator. However, one skilled in the art would recognize that control registers and counters are not comparators. For example, the Microsoft Computer Dictionary defines a comparator as "a device for comparing two items to determine whether they are equal. In electronics, for example, a comparator is a circuit that compares two input voltages and indicates which is higher" (a copy of the title page, bibliographic information, and definitions cited from the Microsoft Computer Dictionary are included as Exhibit A) Exhibit A is being offered in response to the new argument presented in the Final Office Action mailed 6/16/2005. The control register of Levine fails to compare data to each other. It is unclear how a control register that selects an event to count is the same as the presently claimed first comparator circuit. Levine fails to teach or suggest a first comparator circuit as presently claimed.

Therefore, the presently claimed invention is fully patentable over the references and the rejection should be withdrawn.

Levine also fails to teach or suggest a full system monitor configured to monitor and calculate a frequency of use of each bit in the one or more hardware and firmware registers. In particular, Levine is silent in calculating a frequency of use for each bit. The Office Action asserts that "[a] timer based facility may be used to calculate frequency of bits counted" (see Office Action, page 10). However, Levine provides no support for such an assertion. Levine merely teaches that the time based facility 52 which includes a counter designates a precise point in time for saving the machine state. (Levine, column 9, lines 15-18). Levine further states that the time based facility 52 includes **a clock with a frequency** which is based on a system bus clock to provide a synchronized time base (Levine, column 9, lines 19-23). The frequency of Levine is related to a system bus clock. There is nothing in Levine to support the assertion made in the Office Action that Levine teaches or suggests the presently claimed full system monitor configured to monitor and calculate a frequency and use of each bit. Therefore, the presently claimed invention is fully patentable over Levine and the rejection should be withdrawn.

Applicant's representative respectfully requests that the amendment to claim 1 is entered in this after final amendment. The

subject matter added to claim 1 was present in claim 17. As such, no new issues are believed to be raised.

Additionally, claim 12 is independently patentable over Levine. Levine fails to teach or suggest the presently claimed register-delta which comprises a difference between a previous value and a current value registered at one or more of the hardware or firmware registers. Levine merely adjusts the values of performance monitor counts by setting the values **high enough** so that an exception is signaled by some pre-determined number of occurrences of an event (see Levine, column 10, lines 28-32 (emphasis added)). Levine fails to teach the presently claimed register-delta which comprises a **difference** between a previous value and a current value registered at one or more hardware or firmware registers. No reference to the presently claimed register-delta which comprises a difference between a previous value and a current value has been cited in Levine. In particular, it is unclear how the cited section in Levine "...intervals of time may be used to correlate the different samples and different times" supports the assertion that Levine teaches or suggests the presently claimed register-delta (see Office Action, page 9). Levine fails to teach or suggest a register-delta that comprises a difference between a previous value and a current value registered at one or more hardware and firmware registers. Therefore, the

presently claimed invention is fully patentable over Levine and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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